SEC.506

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

Byoung-taek Lee et al.

Group Art Unit: 2823

Serial No.: 09/276,803

Examiner: N. Berezny

Filed: March 26, 1999

For: METHOD FOR MANUFACTURING CAPACITOR OF SEMICONDUCTOR DEVICE HAVING DIELECTRIC LAYER OF HIGH DIELECTRIC CONSTANT

SUPPLEMENTAL RESPONSE SUBMITTING TYPED MARKED-UP VERSION OF CHANGES MADE

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Date: November 13, 2001

Sir:

In response to the Office Action dated October 24, 2001, the following remarks and enclosures are respectfully submitted in connection with the above-identified application.

REMARKS

Claims 1-5 and 7-20 are pending in the present application.

In the Office Action dated October 24, 2001, the Examiner alleged that the Amendment filed on August 10, 2001, was non-responsive by reason of being submitted with a hand-written marked-up version of the amendments made, not a typed-up version. The Examiner's non-responsive holding is traversed for the following reasons.

The Examiner has relied upon 37 C.F.R. §1.121 as the basis for the non-responsive holding. However, this regulation does not specifically require that the marked-up version by typed. Particularly, this regulation does not specify the form of the marked-up version. Indeed, any equivalent marking system may be used. Moreover, 37 C.F.R. §1.52 does not specifically refer to marked-up versions of amendments. This is merely an issue of form over substance, and therefore should not render the Amendment filed on October 24, 2001 as non-responsive. Particularly, the marked-up version submitted along with the Amendment does not render the Amendment unintelligible or burdensome to consider.

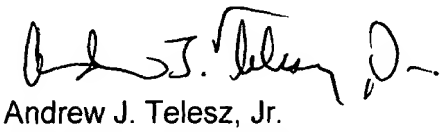
However, in order to expedite prosecution of this application, a typed-up version of the changes made is enclosed. In any event, the Examiner is respectfully requested to examine the application.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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Enclosure: Typed version with marked-up changes

TYPED VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Abstract:

A method [is provided for] of manufacturing a capacitor [of a semiconductor device in which] includes sequentially forming a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer [are sequentially formed] over a semiconductor substrate. [This method includes the steps of performing a] A first post-annealing of the [semiconductor] substrate is performed under an inert atmosphere at a first temperature, and then [performing] a second post-annealing [of the semiconductor substrate] is performed at a second temperature. The first and second post [annealing steps] annealings can be performed after [the deposition] forming the high dielectric layer, the plate electrode, or the interdielectric layer, or any combination [of this] thereof, as long as the second post-annealing [step] is performed after the first post-annealing [step]. The [two] post-[annealing] annealings [steps do not have to be] are not necessarily performed in [the] a same place or [at the same] stage [during the fabrication process]. The first temperature [is preferably in the range of] may be about 600°C to 900°C, and the second temperature [is preferably in the range of] about 100°C to 600°C. [In this way,] As a result, the dielectric constant of the high dielectric layer is increased, and [the] leakage current is reduced.

Additions/Deletions to Claims:

1. (Amended) A method for manufacturing a capacitor of a semiconductor device, comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode over the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature,

the first and second post-annealings being performed in-situ.

9. (Amended) A method for manufacturing a capacitor of a semiconductor device, [as recited in claim 1, wherein] comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode over the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature,

the first and second [post-annealing steps are] post-annealings being performed after the [step of] forming of the plate electrode.

12. (Amended) A method for manufacturing a capacitor of a semiconductor device, [as recited in claim 11, wherein] comprising:

forming a storage electrode over a semiconductor substrate;

forming a high dielectric layer over the storage electrode;

forming a plate electrode over the high dielectric layer;

performing a first post-annealing of the semiconductor substrate under an inert atmosphere at a first temperature;

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature; and

forming an interdielectric layer over the plate electrode,

the first and second [post-annealing steps are] post-annealings being performed after the [step of] forming of the interdielectric layer.

15. (Amended) A method for manufacturing a capacitor of a semiconductor device in which a storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer are sequentially formed on a semiconductor substrate, further comprising:

performing a first post-annealing of the semiconductor substrate under an inert

atmosphere at a first temperature[, after forming one of the high dielectric layer, the plate electrode, and the interdielectric layer]; and

performing a second post-annealing of the semiconductor substrate, after the first post-annealing, at a second temperature lower than the first temperature,

the first and second post-annealings being performed after forming of the plate electrode.